# MIPS Simulator Project Requirement Analysis

**Project 1**

processes an input file

executes the instructions contained in that input file

models their behavior and effect on the processor registers and memory

* non-pipelined fetch-execute architecture
* Fetching an instruction or data item from memory takes 3 cycles
* Executing an instruction in the processor takes 1 cycle
* The execute stage includes the instruction decode operation
* Each instruction may have a different latency depending on the components in the processor’s data path that are used

record how instructions change the machine (computer’s) state.